PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: **Chow, Lap-Wai; et al.**	Examiner: Lee, Eugene
Serial No.: **10/735,841**	Art Unit: 2815
Filed: December 12, 2003	Our Ref: B-4425NP 621267-1
For: "Integrated circuit modification using well implants"	

DECLARATION OF MICHAEL YUNG

United States Patent and Trademark Office
P.O. Box 1450
Arlington, VA 22313-1450

I, Michael Yung, declare as follows:

1. I am not one of the inventors of the subject application. I have a PhD in Electrical Engineering from University of California in Los Angeles and have been working in the field of semiconductor circuits, and in particular the field of Silicon device technology development and integrated circuit design since 1978. I am currently a Research Project Manager at HRL Laboratories in Malibu, California.

2 I am familiar with the Office Action issued on November 21, 2007, and with the Sawada reference (U.S. 5,210,437) cited in this Office Action.

3. I note that in section 4 of the Office Action issued on November 21, 2007, the Examiner rejects claim 1 of the above-referenced application (10/735,841, hereafter the present application) as being anticipated by Sawada.

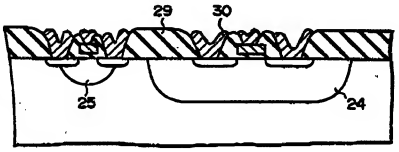
4. I note that the above assertion is inaccurate.

5. Facts about Sawada

6. Sawada's object is (col. 1, line 56-58) to "provide a semiconductor device having different threshold voltages in a plurality of MOS transistors".

7. In particular, Fig. 2E of Sawada (reproduced hereafter) shows a MOS transistor structure having a well 25 forming a channel region between source and drain layers.

FIG. 2E



8. The skilled person understands that when the well 25 is of a conductivity type opposite to that of the source and drain layers, as recited in claim 3 of Sawada, the MOS transistor is an enhancement type MOS transistor.

9. The skilled person understands that when the well 25 is of the same conductivity type as that of the source and drain layers, as recited in claim 2 of Sawada, the MOS transistor is a depletion type MOS transistor.

10. The skilled person knows that in a depletion type MOS transistor, the channel region is rich in carriers and there is an electrical path between the source and drain (i.e. the transistor is ON) until a voltage equal or larger/smaller (for p-channel/n-channel transistor) to a threshold voltage is applied between the source and gate of the transistor, wherein the electric field due to the applied voltage depletes completely the channel region, whereby the electrical path between the source and drain is cut off (i.e. the transistor is OFF).

11. Sawada teaches (col. 1, lines 35-39) that in conventional transistors, "when transistors having different threshold voltages are to be formed, different types of ions

must be implanted in different amounts at different places in order to set different threshold voltages", which leads to a problematic increase of manufacturing process steps if a plurality of threshold voltage is desired.

12. Sawada teaches overcoming the above problem by implanting the channel region of its MOS transistors with "a mask in which a mask pattern width of a portion corresponding to a mask opening diameter is equal to or less than twice the diffusion depth of a well layer" (col. 2, lines 4-7).

13. Sawada teaches that the well formed with such a mask "has a substantially semi-circular section to facilitate impurity concentration control in the surface of the substrate" (col. 2, lines 20-22), because "when a pattern opening diameter is small, the impurity concentration and the depth of a diffusion layer (especially that of an ion-implantation type) are determined by the pattern opening diameter" (col. 3, lines 39-42).

14. Sawada further teaches that "since a plurality of types of opening patterns having a small mask pattern width are formed in a single mask, MOS transistors having different threshold voltages can be formed in a single process" (col. 2, lines 27-30), which is advantageous over the increased number of manufacturing process steps of the prior art of Sawada.

15. Importantly, I note that all of the MOS transistors formed with the masks of Sawada have, as detailed above, a semi-circular section; and that the MOS transistors of Sawada would prima facie look like MOS transistors to a reverse engineer, for example because when looked at from above, they have source and drain regions on both sides of a gate region as generally expected for a MOS transistor.

16. Facts about the structure recited in claim 1

17. Claim 1 recites a camouflaged structure having first and second active regions and having a well with the same type of conductivity as the active regions,

wherein the well is such that it *"provides an electrical path between said first and second active regions regardless of any reasonable voltage applied to said circuit"*."

18. A camouflaged structure such as recited in claim 1 is for example shown in Figure 2 of the present application (reproduced hereafter) wherein a well 7 disposed according to the claimed invention under a gate region and in physical contact with first and second active regions 16a, 18a, provides between the active regions a conductive path regardless of the voltages applied.

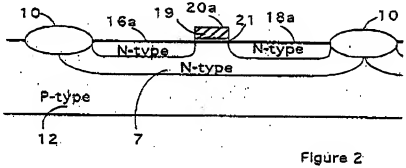


Figure 2

19. The skilled person understands that the above structure would prima facie look like a MOS transistor to a reverse engineer, for example because when looked at from above, it has source and drain regions on both sides of a gate region as generally expected for a MOS transistor.

20. The skilled person understands that because the well 7 has the same type of conductivity as the active regions, a carrier-rich conductive channel, similar in nature to the conductive channel of a depletion transistor, exists in the well 7 between the active regions 16a, 18a.

21. The skilled person further understands that the well 7 has a shape and size such that the carrier-rich conductive channel in the well 7 is very large, and that it is not possible to apply to the structure a reasonable voltage that would generate an electric field strong enough to deplete completely such a large conductive channel.

22. As defined in page 9, lines 10-12 of the application, "a reasonable voltage refers to any gate voltage found in normal device operation such that the voltage does not break down the gate oxide 21".

23. Consequently, and despite the fact that the claimed structure would prima facie look like a MOS transistor to a reverse engineer, the claimed structure is always conductive and does not operate like a MOS transistor.

24. Comparison between the transistor of Sawada and the structure recited in claim 1

25. As outlined above, the transistor of Sawada operates as a MOS transistor and would prima facie look like a MOS transistor to a reverse engineer, whereby the transistor of Sawada is not a "camouflaged circuit structure".

26. On the contrary, the structure recited in claim 1 would prima facie look like a MOS transistor to a reverse engineer but does not operate like a MOS transistor, whereby the structure recited in claim 1 is a "camouflaged circuit structure".

27. At least because of the above reason, I note that Sawada does not disclose or suggest a "camouflaged circuit structure", contrary to claim 1.

28. As also outlined above, a well 25 of the transistor of Sawada "has a substantially semi-circular section" that allows controlling the doping level of the well, and is such that the electrical path between the source and drain regions of the transistor is cut off at a controlled threshold voltage applied to the gate.

29. On the contrary, a well 7 as recited in claim 1 has no semi-circular section, and is such that the electrical path between the active regions of the recited structure is never cut off for any reasonable voltage applied to the circuit, including any reasonable voltage applied to the gate.

30. At least because of the above reason, I note that Sawada does not disclose or suggest a well that "provides an electrical path between said first and second active regions regardless of any reasonable voltage applied to said circuit", as specifically required in claim 1, and therefore claim 1 is not anticipated by Sawada.

* * *

31. I declare that all statements made herein are true, and that all statements made upon information and belief are believed to be true, and further, that these statements were made with the knowledge that willful, false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001, and that willful, false statements may jeopardize the validity of the application, or any patent issuing thereon.

Dated: March 19, 2008 By: Michael Yang
Michael Yang